

AMENDMENT TO THE CLAIMS:

1 - 17 (Cancelled)

18. (Original) A semiconductor device with improved leakage control, comprising:

a P doped semiconductor substrate having a top surface;

a STI in said substrate, said STI having a bottom, a first sidewall and an opposite second sidewall;

a leakage stop implant in said substrate under the bottom of said STI and under and aligned to said second sidewall; and

an N-well in said substrate adjacent to and in contact with said first sidewall, said N-well extending under said STI and forming an upper portion of an isolation junction with said leakage stop implant, said upper portion of said isolation junction located entirely under said STI.

19. (Original) The semiconductor device of claim 18, further comprising a P-well in said substrate adjacent to and in contact with said second sidewall, said P-well incorporated into said upper portion and forming a lower portion of said isolation junction with said N-well.

20. (Original) The semiconductor device of claim 18, wherein said leakage stop implant extends under said STI from said second sidewall toward said first sidewall a distance equal to 10 to 40% of the width of said STI

21. (Original) The semiconductor device of claim 18, wherein the concentration of P dopant at an interface formed by the bottom of said STI and said substrate is $3E16 \text{ atm/cm}^3$ to $1E17 \text{ atm/cm}^3$.

22. (Original) The semiconductor device of claim 21, wherein the concentration of P dopant at about 0.1 micron below said interface under said second sidewall is $1.0E17 \text{ atm/cm}^3$ to $1.5E17 \text{ atm/cm}^3$.

23. (Original) The semiconductor device of claim 18, further comprising spacers on said first and second sidewalls of and contained within said STI.

24. (Original) The semiconductor device of claim 23, wherein said spacers are silicon nitride.

25. (Original) The semiconductor device of claim 18, wherein said STI is filled with TEOS or HDP oxide.

26. (Original) The semiconductor device of claim 25, further including a liner on said bottom, first sidewall and second sidewall of said STI.

27. (Original) The semiconductor device of claim 26, wherein said liner is 10 to 30 nm thick thermal oxide.

28. (Original) The semiconductor device of claim 26, further comprising spacers on said liner over said first and second sidewalls of and contained within said STI

29. (Original) The semiconductor device of claim 19, wherein said STI is 0.05 to 1 micron in depth and 0.1 to 5 microns in width.

30. (Original) The semiconductor device of claim 19, further comprising a PFET in said N-well and an NFET in said P-well.

31-47 (Cancelled)

48. (Original) A semiconductor device with improved leakage control, comprising:
an N doped semiconductor substrate having a top surface;
a STI in said substrate, said STI having a bottom, a first sidewall and an opposite second sidewall;
a leakage stop implant in said substrate under the bottom of said STI and under and aligned to said second sidewall; and
a P-well in said substrate adjacent to and in contact with said first sidewall, said P-well extending under said STI and forming an upper portion of an isolation junction with said leakage stop implant, said upper portion of said isolation junction located entirely under said STI.

49. (Original) The semiconductor device of claim 48, further comprising an N-well in

said substrate adjacent to and in contact with said second sidewall, said N-well incorporated into said upper portion and forming a lower portion of said isolation junction with said P-well.

50. (Original) The semiconductor device of claim 48, wherein said leakage stop implant extends under said STI from said second sidewall toward said first sidewall a distance equal to 10 to 40% of the width of said STI

51. (Original) The semiconductor device of claim 48, wherein the concentration of N dopant at an interface formed by the bottom of said STI and said substrate is $3\text{E}16 \text{ atm/cm}^3$ to $1\text{E}17 \text{ atm/cm}^3$.

52. (Original) The semiconductor device of claim 51, wherein the concentration of N dopant at about 0.1 micron below said interface under said second sidewall is $1.0\text{E}17 \text{ atm/cm}^3$ to $1.5\text{E}17 \text{ atm/cm}^3$.

53. (Original) The semiconductor device of claim 48, further comprising spacers on said first and second sidewalls of and contained within said STI.

54. (Original) The semiconductor device of claim 53, wherein said spacers are silicon nitride.

55. (Original) The semiconductor device of claim 48, wherein said STI is filled with

TEOS or HDP oxide.

56. (Original) The semiconductor device of claim 55, further including a liner on said bottom, first sidewall and second sidewall of said STI.

57. (Original) The semiconductor device of claim 56, wherein said liner is 10 to 30 nm thick thermal oxide.

58. (Original) The semiconductor device of claim 56, further comprising spacers on said liner over said first and second sidewalls of and contained within said STI

59. (Original) The semiconductor device of claim 49, wherein said STI is 0.05 to 1 micron in depth and 0.1 to 5 microns in width.

60. (Original) The semiconductor device of claim 49, further comprising an NFET in said P-well and a PFET in said N-well.

REMARKS

Favorable consideration and allowance of the claims of the present application, as amended herein, is respectfully requested.

In this preliminary amendment, applicants have cancelled original Claim 1-17 and 31-47. Applicants have also amended the specification to include reference to the parent application.

Since the above amendments to the claims and specification do not introduce new matter

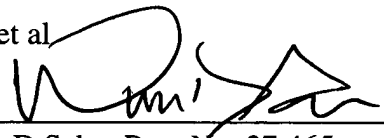
into the application, entry thereof is respectfully requested.

Consideration and allowance of the claims of the present application are thus respectfully requested.

Respectfully submitted,

FOR: Logan, et al

BY:


William D. Sabo, Reg. No. 27,465

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IBM Corporation
1000 River Street, 972E
Essex Junction, VT 05452
(802)769-9454